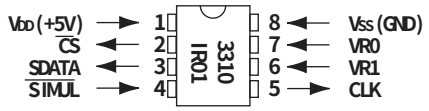
CS3310/PGA2310 stand-alone controller
(International Rectifier Japan version 01)

Output Command Range

TACHYONIX3310IR01 Gain Range specialized for IRAUDAMP3
Control Voltage 0～VDD(+5V) → MUTE～ +15.0dB

Pin Configration



Note: Vdd and Vss are located on the other side compared with usual Logic ICs.

Package

- 8pin Plastic DIP 300 mil

Absolute Maximum Rainings

Temperature Under Bias	-40℃～+125℃
Storage Temperature	-65℃～+150℃
Input Voltage	-0.3V～VDD+0.3V
Supply Voltage VDD	-0.3～+6.5V
Input Clamp Current	± 20mA
Maximum Sink Current	25mA
Maximum Source Current	25mA

Operating Condition

Supply Voltage VDD	4.75～5.25 (5.0 Typ.) V
	IDD < 2mA Max
Temperature Range	0℃～+70℃

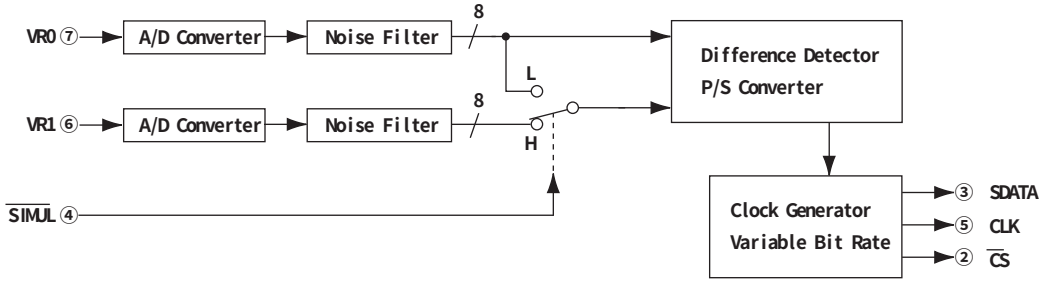
Note: All temperature ranges are specified only for the chip. But the product number label can endure under normal soldering oparation.

Pin Assignments

PIN	NAME	I/O	F U N C T I O N
1	VDD	Power	Positive Supply,+5V(typ.)
2	$\overline{CS}$	O	Chip Select Output (Directly connectable to CS3310/PGA2310 $\overline{CS}$)
3	SDATA	O	Serial Data Output (Directly connectable to CS3310 SDATAI/PGA2310 SDI)
4	$\overline{SIMUL}$	I	Simultaneous Mode Select Input (Active LOW,TTL Threshold) H=Independent Mode,L=Simultaneous Mode
5	CLK	O	Serial Clock Output (Directly connectable to CS3310/PGA2310 SCLK)
6	VR1	I	Gain Control Input for Daisy-Chained CS3310/PGA2310 0～VDD(+5V) → MUTE～ +15.0dB (Recommended Source Impedance is 10kΩ or less)
7	VR0	I	Gain Control Input for Directly connected CS3310/PGA2310 0～VDD(+5V) → MUTE～ +15.0dB (Recommended Source Impedance is 10kΩ or less)
8	VSS	Power	Ground Reference(GND)

※ Please refer to 3310S**S Japanese version data sheets for details.

Internal Processing Diagram



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